REMARKS

By the foregoing amendment, the specification has been amended to update one of the priority application citations in the cross-reference section; and claims 1, 9, 12-14, 17, 20-22, 25, 33, 39, 41, and 42 have been amended to correct clerical errors. Marked-up versions of the amended specification section and the amended claims are provided in the attached Appendix.

In the Office Action, the disclosure was objected to for not listing in the cross-reference section U.S. Patent No. 6,357,665 — the patent that issued from the parent application; claims 1-44 were rejected under 35 U.S.C. § 102(b) as being anticipated by Shinagawa (U.S. Patent No. 5,126,541); and claims 1-44 were further rejected for obviousness-type double patenting over claims 1-48 of U.S. Patent No. 6,357,665 — the aforementioned patent that issued from the parent application.

With regard to the objection to the disclosure, the cross-reference section has now been amended to refer to U.S. Patent No. 6,357,665, which issued from the parent application subsequent to the filing of this continuation application. It is therefore believed that the objection to the disclosure has been overcome.

With regard to the § 102(b) rejections of claims 1, 9, and 17 over Shinagawa, each of these claims recites the following features: (1) the manufacture of an IC card includes storage of programming instructions, but does not include storage of an address table with memory addresses of at least one of the programming instructions; and (2) the aforementioned address table is stored on the card during personalization of the card. With regard to the first feature, applicants have carefully reviewed the Shinagawa reference, particularly the sections cited on page 2 of the Office Action (col. 3, ln. 50 -

col. 4, ln. 21; and col. 7, ln. 60 - col. 8, ln. 3), and are unable to find any mention or suggestion of an IC card which is manufactured with programming instructions but without an address table with memory addresses of at least one of the programming instructions. In particular, there is only one program stored on the Shinagawa card during the manufacturing process: the system program, a/k/a the basic processing program. *See* col. 3, lns. 50-52. It is apparent from the reference that the system program is immediately operational after the card is manufactured, because the manufactured card is ready to receive the application program during the issuing process. *See* col. 3, lns. 52-58 and 61-64. It is therefore clear that, once the card has been manufactured, it already contains any and all memory addresses of programming instructions included in the system program. In other words, the Shinagawa system lacks the feature of manufacturing a card without an address table with memory addresses of at least one of the programming instructions stored on the card at the time of manufacture.

As for the storage of the address table on the card during personalization, applicants are also unable to find any mention or suggestion of this second feature anywhere in Shinagawa, particularly in the sections cited in the Office Action (col. 3, ln. 50 - col. 4, ln 21; and col. 7, ln. 60 - col. 8, ln. 3). Furthermore, as is discussed above, the system program is the only program stored on the Shinagawa card during manufacture. As a result, because all necessary memory addresses are already on the Shinagawa card once the card has been manufactured, there would be no reason — based on the teachings of the cited reference — for storing during personalization an address table with memory addresses of at least one of the programming instructions in the system program. It is

therefore not surprising that the Shinagawa system lacks the additional feature of storing such an address table during personalization.

In addition, unlike the present application, the Shinagawa reference provides no motivation for providing a card system with the above-described features of claims 1, 9, and 17 of the present application. As is stated on page 11, ¶00030 of the specification, a benefit of the present invention is that it allows the system to use a card "despite an outdated codelet or primitive which may have been permanently placed in the card at the time of manufacture." In contrast, the methods taught in the cited reference are for the purposes of debugging, developing, and evaluating applications to be executed on IC Cards (*see* col. 2, lns. 25-35; col. 4, lns. 40-57; col. 5, ln. 66 - col. 6, ln. 1; and col. 6, lns. 6 - 48), and are completely unrelated to enabling the use of a card despite an outdated codelet or primitive remaining on the card. Shinagawa makes no mention or suggestion of outdated codelets or primitives, much less whether it would be beneficial to use a card having such outdated codelets or primitives. Accordingly, it is clear that the present invention as recited in claims 1, 9, and 17 is neither anticipated nor rendered obvious by Shinagawa.

With regard to the § 102(b) rejections of claims 2, 5, 10, 13, 18, and 21 over Shinagawa, it is first noted that claims 2 and 5 ultimately depend from allowable claim 1; claims 10 and 13 ultimately depend from allowable claim 9; and claims 18 and 21 ultimately depend from allowable claim 17. Furthermore, each of the aforementioned dependent claims recites the further limitation of programming instructions which comprise at least one primitive. Applicants are unable to find any mention of primitives anywhere in the cited reference, Shinagawa, and in fact, the section cited on page 2 of the

Office Action (col. 5, lines 16-25) merely describes a "debugger program [which] sets to [a] data memory ... address information items and the like" to be used in a data output section, a program initiate section, and a program stop section. The data output section, the program initiate section, and the program stop section are then initiated by generating operation enable signals. Shinagawa does not state or even suggest that the aforementioned sections are primitives. As is stated on page 3, ¶ 0006 of the present application, "Primitives are written in native language (i.e. assembler language) so that they can be executed very quickly and minimal interpretation of the instructions is necessary for execution." Shinagawa fails to provide any such description or even use the word "primitive." Furthermore, there is nothing in Shinagawa which would suggest that the data output section, the program initiate section, or the program stop section are, or should be, primitives. It is therefore clear that the additional limitations recited in claims 2, 5, 10, 13, 18, and 21 of the present invention are neither anticipated nor rendered obvious by the cited reference. Accordingly, because these claims depend from allowable independent claims, and recite further novel and non-obvious limitations, claims 2, 5, 10, 13, 18, and 21 should be allowed.

With regard to the § 102(b) rejections of claims 3, 6, 11, 14, 19, and 22 over Shinagawa, it is first noted that claims 3 and 6 ultimately depend from allowable claim 1; claims 11 and 14 ultimately depend from allowable claim 9; and claims 19 and 22 ultimately depend from allowable claim 17. Furthermore, each of the aforementioned dependent claims recites the further limitation of programming instructions which comprise at least one codelet. Applicants are unable to find any mention of codelets anywhere in Shinagawa, and in particular, the figure and section cited on page 2 of the

Office Action (figure 5 and col. 5, lines 12-16) have nothing to do with storing codelets in the memory of a card. The cited section of Shinagawa merely discusses switching a mode of a card to a "development mode," and initiating a debugger program. Furthermore, Applicants are unable to find any indication, anywhere in the cited reference, that storing a codelet would be useful for switching a card to a development mode and initiating a debugger program. It is therefore clear that the cited reference neither teaches nor renders obvious the additional limitations recited in claims 3, 6, 11, 14, 19, and 22. Accordingly, because these dependent claims depend from allowable base claims, and recite further novel and non-obvious limitations, claims 3, 6, 11, 14, 19, and 22 should be allowed.

With regard to the § 102(b) rejections of claims 7, 8, 15, 16, 23, and 24 over Shinagawa, it is first noted that claims 7 and 8 ultimately depend from allowable independent claim 1; claims 15 and 16 ultimately depend from allowable independent claim 9; and claims 23 and 24 ultimately depend from allowable independent claim 17. In addition, claims 7, 8, 15, 16, 23, and 24 depend from allowable dependent claims 5, 6, 13, 14, 21, and 22, respectively. Furthermore, claims 7, 15, and 23 recite the additional limitation of an address table which comprises a listing of names and addresses of primitives; and claims 8, 16, and 24 recite the additional limitation of an address table which comprises a listing of names and addresses of codelets. In contrast, the cited reference fails to teach such limitations. In particular, Applicants are unable to find any mention or suggestion, anywhere in the cited reference, of the storage of the name of a programming instruction in an address table. As for Figure 1 of Shinagawa, which is cited on page 2 of the Office Action, this drawing fails to disclose any name associated

with programming instructions stored in a table. In addition, Shinagawa does not disclose or suggest any reason why the storage of a name of a set of programming instructions would be of any use or benefit for the mode-switching and debugging techniques discussed in the reference. It is therefore clear that the cited reference fails to disclose or render obvious the additional limitations of claims 7, 8, 15, 16, 23, and 24 of the present invention. Accordingly, because each of these claims depends from allowable claims and recites further novel and non-obvious limitations, claims 7, 8, 15, 16, 23, and 24 are also allowable.

With regard to the § 102(b) rejections of claims 4, 12, and 20 over Shinagawa, these dependent claims depend from independent claims 1, 9, and 17, respectively, which are allowable, as is discussed above. Accordingly, claims 4, 12, and 20 should also be allowed.

With regard to the § 102(b) rejections of claims 25, 33, and 39 over Shinagawa, each of these claims recites the feature of personalizing an IC card after the time of manufacture and storing at the time of personalization an address table with memory addresses of at least one of the programming instructions that were stored at the time of manufacture. In contrast, no such feature is anywhere to be found in Shinagawa, the cited reference. In particular, the sections of the reference cited on page 2 of the Office Action (col. 3, ln. 50 - col. 4, ln. 21; and col. 7, ln. 60 - col. 8, ln. 3) make no mention of such a feature. In fact, as is discussed above in the context of claims 1, 9, and 17, the system program is the only program stored on the Shinagawa card during the manufacturing process (*see* col. 3, lns. 50-52), and once the card has been manufactured, it already contains any memory addresses needed to access the programming instructions

in the system program. Accordingly, Shinagawa provides no motivation for storing such addresses during personalization of a card. Furthermore, as is also discussed above with respect to claims 1, 9, and 17, a benefit of the present invention is that it allows a system to use a card "despite an outdated codelet or primitive which may have been permanently placed in the card at the time of manufacture." *See* specification, page 11, ¶ 00030. In contrast, there is nothing in Shinagawa which even mentions the use of a card despite an outdated codelet or primitive, much less any technique which would enable the use of a card containing any outdated programming instructions. Accordingly, Shinagawa cannot either anticipate or render obvious the present invention according to claims 25, 33, and 39.

With regard to the §102(b) rejections of claims 26, 34, and 40 over Shinagawa, it is first to be noted that these claims depend from claims 25, 33, and 39, respectively. In addition, the present invention according to claims 26, 34, and 40 includes the following features: (1) the storage of additional programming instructions corresponding to updated versions of previously stored or existing programming instructions; and (2) inserting addresses in an address table by overwriting existing addresses with the addresses of the corresponding updated programming instructions. Applicants are unable to find any such features anywhere in Shinagawa, the cited reference. In particular, the section cited on page 2 of the Office Action (col. 4, lines 44-48) merely refers to the loading of debug processing data including information to specify an initiating position or an execution start address of an application program. No mention is made of either: (1) updated versions of previously stored programming instructions, or (2) overwriting existing addresses with addresses of the corresponding

updated programming instructions. In fact, there is nothing in Shinagawa which would provide any motivation for such features, and accordingly, the additional subject matter recited in claims 26, 34, and 40 cannot be either anticipated or rendered obvious by the cited reference. Therefore, because claims 26, 34, and 40 depend from allowable claims, and recite further novel and non-obvious subject matter, the present invention according to claims 26, 34, and 40 is also patentable over Shinagawa.

With regard to § 102(b) rejections of claims 27, 29, 35, and 41 over Shinagawa, it is first noted that claims 27 and 29 ultimately depend from allowable claims 25 and 26; claim 35 depends from allowable claims 33 and 34; and claim 41 depends from allowable claims 39 and 40. Furthermore, each of claims 27, 29, 35, and 41 recites the additional limitation of programming instructions which comprise at least one primitive. As is discussed above with respect to claims 2, 5, 10, 13, 18, and 21, this limitation is neither disclosed nor rendered obvious by Shinagawa. Accordingly, since each of claims 27, 29, 35, and 41 depends from allowable claims, and recites a further novel and non-obvious limitation, claims 27, 29, 35, and 41 should also be allowed.

With regard to the § 102(b) rejections of claims 28, 30, 36, and 42 over Shinagawa, it is first noted that claims 28 and 30 ultimately depend from allowable claims 25 and 26; claim 36 depends from allowable claims 33 and 34; and claim 42 depends from allowable claims 39 and 40. Furthermore, each of claims 28, 30, 36, and 42 recites the additional limitation of programming instructions which comprise at least one codelet. As is discussed above with respect to claims 3, 6, 11, 14, 19, and 22, this limitation is neither disclosed nor rendered obvious by Shinagawa. Accordingly, because

each of claims 28, 30, 36, and 42 depends from an allowable claim, and recites a further novel and non-obvious limitation, claims 28, 30, 36, and 42 should be allowed.

With regard to the § 102(b) rejections of claims 31, 32, 37, and 38 over Shinagawa, it is first noted that claims 31 and 32 ultimately depend from allowable claims 25 and 26, and claims 37 and 38 ultimately depend from allowable claims 33 and 34. In addition, claims 31 and 32 depend from allowable claims 27 and 28, respectively, and claims 37 and 38 depend from allowable claims 35 and 36, respectively. Claims 31 and 37 also recite the limitation of an address table which comprises a listing of names and addresses of primitives. As is discussed above with respect to claims 7, 15, and 23, this additional feature is neither anticipated nor rendered obvious by Shinagawa. As for claims 32 and 38, each of these claims recites the further limitation of an address table which comprises a listing of names and addresses of codelets. As is discussed above with respect to claims 8, 16, and 24, this additional feature is also neither anticipated nor rendered obvious by the cited reference. Accordingly, because claims 31, 32, 37, and 38 depend from allowable claims and recite further novel and non-obvious limitations, claims 31, 32, 37, and 38 are also allowable.

With regard to the § 102(b) rejections of claims 43 and 44 over Shinagawa, each of these claims recites the following features: (1) manufacturing an IC card and storing at the time of manufacture in the IC card a first set of programming instructions having a first address, without an address table with a second memory address of a second set of programming instructions; (2) storing in the IC card the second set of programming instructions; and (3) storing in the IC card, at a time of personalization, the address table with the second memory address, wherein after the time

of personalization, the first set of programming instructions is rendered inaccessible to the operating system. Applicants have carefully reviewed the Shinagawa reference, particularly the sections cited on page 2 of the Office Action (col. 3, line 50 - col. 4, line 21; and col. 7, line 60 - col. 8, line 3), and are unable to find any mention or suggestion of the aforementioned features in the cited reference. Moreover, as is discussed above with respect to claims 1, 9, and 17, the purposes of the Shinagawa system are debugging, developing, and evaluating applications to be executed on IC cards (*see* col. 2, lns. 25-35; col. 4, lns. 40-57; col. 5, ln. 66 - col. 6, ln. 1; and col. 6, lns. 6-48), and the cited reference therefore provides no motivation for employing the aforementioned features of the present invention according to claims 43 and 44. For example, there is no mention or suggestion of rendering any set of programming instructions inaccessible after personalization of the Shinagawa card, nor does the reference provide any reason for such a feature.

In addition, applicants point out that the same reference — Shinagawa — was also the sole reference at issue in the parent application, Serial No. 09/162,605. Applicants therefore respectfully refer the Examiner to the following language in his reasons for allowance set forth on page 2 of the July 30, 2001 Notice of Allowability in the parent application:

> The applicant teaches a multiple application card system having a manufacturing process wherein the manufacturing process includes storing a first set of programming instructions having a first address, without an address table and storing a second set of programming instructions having a second address and an address table, wherein the first programming instructions are not accessible by the operating system. These limitations in conjunction with other limitations of the independent and dependent claims were not shown by the prior art.

Applicants respectfully request that the Examiner consider the features recited in currently pending claims 43 and 44 in view of the above-cited reasons for allowance in the parent case. It is believed that the above-cited reasons for allowance make it even more apparent that claims 43 and 44 are allowable over Shinagawa.

Applicants submit that the foregoing discussion of claims 43 and 44 demonstrates that these claims recite subject matter which is novel and non-obvious over the Shinagawa reference, and that these claims should therefore be allowed.

With regard to the double patenting rejection of claims 1-44, applicants submit herewith a terminal disclaimer under 37 C.F.R. § 1.321 disclaiming the terminal part of any patent term extending beyond the expiration date of U.S. Patent No. 6,357,665, which issued from the parent application. It is believed that the double patenting rejection of claims 1-44 has thus been overcome.

Accordingly, in light of the foregoing discussion, it is submitted that claims 1-44, all of the pending claims, are in condition for allowance. Favorable reconsideration of these claims is therefore respectfully requested.

Respectfully submitted,

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APPENDIX A

VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph 0001 of the specification has been amended as follows:

This application is a continuation of United States Patent Application Serial No. 09/162,605 filed on September 29, 1998, now Patent No. 6,357,665, entitled "Configuration of IC Card," which claims priority to United States Provisional Application Serial No. 60/073,906 filed on February 6, 1998, entitled "Remote Configuration of IC Card," and United States Provisional Application Serial No. 60/072,561, filed on January 22, 1998, entitled "Codelets," all of which are incorporated herein by reference.

In the Claims:

Claims 1, 9, 12-14, 17, 20-22, 25, 33, 39, 41, and 42 have been amended as follows:

1. (Amended) A secure multiple application card system including an IC card comprising a microprocessor, a read-only memory and an electrically erasable programmable read only memory, said system comprising:

means for manufacturing said IC card and for storing at the time of manufacture in said read-only memory an operating system and programming instructions without an address table with memory addresses of at least one of said programming instructions; and

means for personalizing said IC card after said manufacturing step and for storing at the time of personalization in said electrically erasable programmable read only

memory said address table with memory addresses of at least one of said programming instructions,

wherein the operating system will only access those programming instructions in accordance with the addresses indicated in the address table.

9. (Amended) A process for providing a secure multiple application card system including an IC card comprising a microprocessor, a read-only memory and an electrically erasable programmable read only memory, said process comprising the steps of:

manufacturing said IC card and [for] storing at the time of manufacture in said read-only memory an operating system and programming instructions without an address table with memory addresses of at least one of said programming instructions; and

personalizing said IC card after said time of manufacture by storing in said electrically erasable programmable read only memory said address table with memory addresses of at least one of said programming instructions,

wherein the operating system will only access those programming instructions in accordance with the addresses indicated in the address table.

12. (Amended) The process of claim 9, wherein said step [for] of storing in said electrically erasable programmable read only memory further includes storing additional programming instructions.

13. (Amended) The process of claim 12, wherein said additional programming instructions comprise[s] at least one primitive.

14. (Amended) The process of claim 12, wherein said additional programming instructions comprise[s] at least one codelet.

17. (Amended) A process for providing a secure multiple application card comprising a microprocessor, a first memory and a second memory, said process comprising the steps of:

manufacturing said card and storing at the time of manufacture in said first memory an operating system and programming instructions without an address table with memory addresses of at least one of said programming instructions; and

personalizing said IC card after said storing step by storing in said second memory said address table with memory addresses of at least one of said programming instructions;

wherein said operating system will only access those programming instructions in accordance with the addresses indicated in the address table.

20. (Amended) The process of claim 17, wherein said step [for] of storing in said electrically erasable programmable read only memory further includes storing additional programming instructions.

21. (Amended) The process of claim 20, wherein said additional programming instructions comprise[s] at least one primitive.

22. (Amended) The process of claim 20, wherein said additional programming instructions comprise[s] at least one codelet.

25. (Amended) A secure multiple application card system including an IC card comprising a microprocessor, a read-only memory and an electrically erasable programmable read only memory, said system comprising:

means for manufacturing said IC card and for storing at the time of manufacture in said read-only memory an operating system and programming instructions; and

means for personalizing said IC card after the time of manufacture and for storing at the time of personalization in said electrically erasable programmable read only memory an address table with memory addresses of at least one of said programming instructions,

wherein the operating system will only access those programming instructions in accordance with the addresses indicated in the address table;

and wherein said means for personalizing said IC card can be operated to store additional programming instructions in said read-only memory and includes means for inserting addresses for said additional programming instructions in said address table.

33. (Amended) A process for providing a secure multiple application card system including an IC card comprising a microprocessor, a read-only memory and an electrically erasable programmable read only memory, said process comprising the steps of:

manufacturing said IC card and [for] storing at the time of manufacture in said read-only memory an operating system and programming instructions; [and]

personalizing said IC card after said time of manufacture by storing in said electrically erasable programmable read[-]only memory an address table with memory

addresses of at least one of said programming instructions,

wherein the operating system will only access those programming instructions in accordance with the addresses indicated in the address table;

storing additional programming instructions in said read-only memory[,]; and

inserting addresses for said additional programming instructions in said address table.

39. (Amended) A process for providing a secure multiple application card comprising a microprocessor, a first memory and a second memory, said process comprising the steps of:

a. storing in said first memory an operating system and programming instructions; [and]

b. personalizing said IC card after said storing step by storing in said second memory an address table with memory addresses of at least one of said programming instructions[;],

wherein said operating system will only access those programming instructions in accordance with the addresses indicated in the address table;

c. storing additional programming instructions in said read-only memory[, said]; and

d. inserting addresses for said additional programming instructions in said address table.

41. (Amended) The process of claim 40, wherein said programming instructions comprise[s] at least one primitive.

42. (Amended) The process of claim 40, wherein said programming instructions comprise[s] at least one codelet.